

1. A bus framer comprising:

an engine which extracts information from a frame of data being transmitted over a time-division multiplexed bus; and
a processor which retrieves the information from the
5 engine over an internal bus and forwards the information.

2. The bus framer of claim 1, further comprising:

a mapper which maps the frame of data on the time-division multiplexed bus to a read/write bus; and
a functional module which receives data from the
read/write bus and which handles the data.

3. The bus framer of claim 2, wherein the time-division multiplexed bus, the internal bus, and the read/write bus all run off the same clock.

4. The bus framer of claim 1, further comprising:
a storage medium for storing the information in a database; and

20 an interface module which provides a link to an external device;
wherein the processor forwards the information to at least one of the storage medium and the interface module.

5. The bus framer of claim 1, further comprising:
a framing engine which generates the frame and outputs
the frame to the time-division multiplexed bus.

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6. The bus framer of claim 5, wherein the framing engine
stores the frame in memory prior to outputting the frame, the
frame in memory comprising:

10 a data structure having blocks arranged in N rows and M
columns, where N and M are integers that are greater than one,
a block including data corresponding to a destination port and
a time slot for the data.

15 7. The bus framer of claim 1, wherein the engine
comprises one of (a) a signaling engine which extracts
signaling information from the frame, (b) an alarms engine
which extracts alarm codes from the frame, (c) a facility data
link engine which extracts messages from the frame, and (d) an
overhead engine which extracts overhead bits from the frame.

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8. The bus framer of claim 2, wherein the functional
module comprises one of (a) a scalar high-speed bus, (b) a
slip buffer which stores data temporarily to accommodate

frequency and phase differences between a clock of the bus framer and external clock domains, (c) a system backplane with a connection to an external device, (d) a bit error rate testing generator/analyizer, and (e) a high-speed data link controller.

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9. The bus framer of claim 1, further comprising:

a read/write bus;
plural functional modules which communicate with the
engine via the read/write bus; and
an arbiter which regulates access of the plural
functional modules to the read/write bus.

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10. The bus framer of claim 9, wherein the arbiter
grants a first of the plural functional modules access to the
read/write bus in a first bus cycle, and grants a second of
the plural functional modules access to the read/write bus in
a second bus cycle, the second bus cycle immediately following
the first bus cycle.

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11. A method comprising:

using an engine to extract information from a frame of
data being transmitted over a time-division multiplexed bus;
and

5 retrieving the information from the engine over an
internal bus and forwarding the information.

12. The method of claim 11, further comprising:

mapping the frame of data on the time-division
multiplexed bus to a read/write bus; and

forwarding the frame of data, over the read/write bus, to
a functional module which handles the data.

13. The method of claim 12, wherein the time-division
multiplexed bus, the internal bus, and the read/write bus all
run off the same clock.

14. The method of claim 11, further comprising:

storing the information in a database on a storage
medium;

wherein the information is forwarded to at least one of
the storage medium and an external device.

15. The method of claim 11, further comprising:
generating the frame; and
outputting the frame to the time-division multiplexed
bus.

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16. The method of claim 15, further comprising
storing the frame in memory prior to outputting the frame, the
frame in memory comprising:

a data structure having blocks arranged in N rows and M
columns, where N and M are integers that are greater than one,
a block including data corresponding to a destination port and
a time slot for the data.

17. The method of claim 11, wherein the engine comprises
one of (a) a signaling engine which extracts signaling
information from the frame, (b) an alarms engine which
extracts alarm codes from the frame, (c) a facility data link
engine which extracts messages from the frame, and (d) an
overhead engine which extracts overhead bits from the frame.

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18. The method of claim 12, wherein the functional
module comprises one of (a) a scalar high-speed bus, (b) a
slip buffer which stores data temporarily to accommodate

frequency and phase differences between an internal clock and external clock domains, (c) a system backplane with a connection to an external device, (d) a bit error rate testing generator/analyizer, and (e) a high-speed data link controller.

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19. The method of claim 11, further comprising:
regulating access of plural functional modules to a read/write bus over which communications are exchanged with the engine.

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20. The method of claim 19, wherein regulating comprises:

granting a first of the plural functional modules access to the read/write bus in a first bus cycle; and

granting a second of the plural functional modules access to the read/write bus in a second bus cycle, the second bus cycle immediately following the first bus cycle.

21. An article comprising a machine-readable medium that stores executable instructions, the instructions causing a machine to:

extract information from a frame of data being transmitted over a time-division multiplexed bus; and

retrieve the information over an internal bus and forward the information.

22. The article of claim 21, further comprising
5 instructions to:

map the frame of data on the time-division multiplexed bus to a read/write bus; and
forward the frame of data, over the read/write bus, to a functional module which handles the data.

23. The article of claim 22, wherein the time-division multiplexed bus, the internal bus, and the read/write bus all run off the same clock.

24. The article of claim 21, further comprising
instructions to:

store the information in a database on a storage medium; wherein the information is forwarded to at least one of the storage medium and an external device.

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25. The article of claim 21, further comprising
instructions to:

generate the frame; and

output the frame to the time-division multiplexed bus.

26. The article of claim 25, further comprising
instructions to store the frame in memory prior to outputting
5 the frame, the frame in memory comprising:

a data structure having blocks arranged in N rows and M
columns, where N and M are integers that are greater than one,
a block including data corresponding to a destination port and
a time slot for the data.

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27. The article of claim 21, wherein the information is
extracted using an engine, the engine comprising one of (a) a
signaling engine which extracts signaling information from the
frame, (b) an alarms engine which extracts alarm codes from
the frame, (c) a facility data link engine which extracts
messages from the frame, and (d) an overhead engine which
extracts overhead bits from the frame.

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28. The article of claim 22, wherein the functional
module comprises one of (a) a scalar high-speed bus, (b) a
slip buffer which stores data temporarily to accommodate
frequency and phase differences between an internal clock and
external clock domains, (c) a system backplane with a

connection to an external device, (d) a bit error rate testing generator/analyizer, and (e) a high-speed data link controller.

29. The article of claim 21, further comprising
5 instructions to:

regulate access of plural functional modules to a
read/write bus over which communications are exchanged with
the engine.

10 30. The article of claim 29, wherein regulating
comprises:

granting a first of the plural functional modules access
to the read/write bus in a first bus cycle; and

15 granting a second of the plural functional modules access
to the read/write bus in a second bus cycle, the second bus
cycle immediately following the first bus cycle.